CMC110

Energy Measurement IC for Single-Phase Energy Metering Application

Features

- Energy Measurement Accuracy of 0.1% over 1000:1 Dynamic Range
- Two 24-bit 3rd-order ΣΔ Modulators for Voltage and Current Measurements
- Two high Gain PGAs with a Range of up to x32
- Supports Current Transformer (CT) and Shunt Resistor
- On-Chip Computation Engine
  - Active/Reactive/Apparent Power and Energy
  - RMS Voltage and Current
  - Power Factor and Line Frequency
- Monitors electric conditions such as Voltage Sag , Voltage Swell, and Over-current
- On-Chip Calibration Functionality
- UART, I2C and SPI Serial Interface
- Single 3.3 V Power Supply.
- Low Power Consumption : <15mW
- 32-pin QFN package (5 mm x 5 mm)

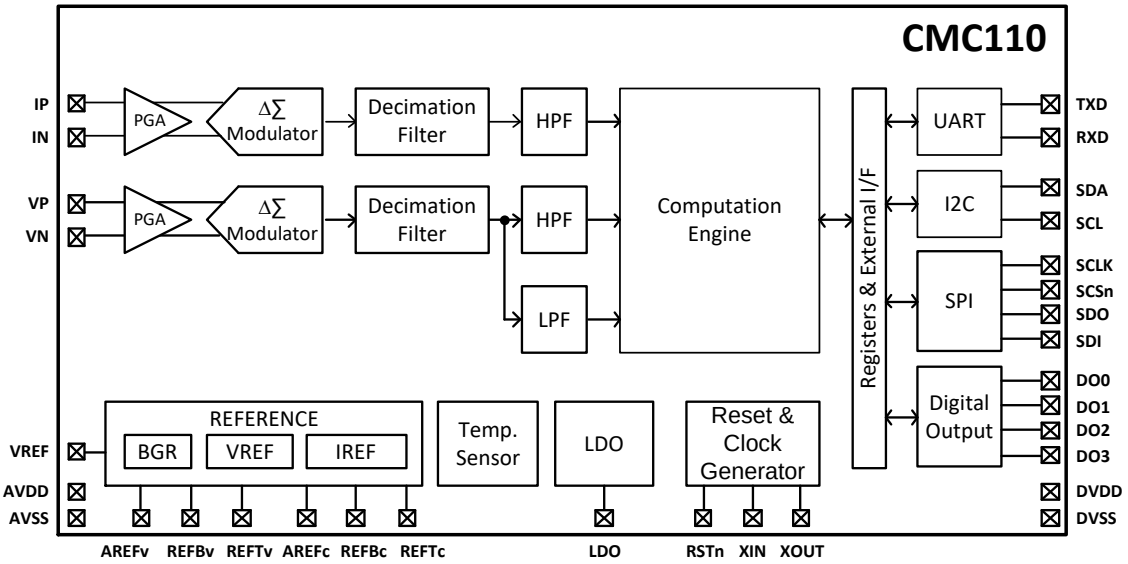
General Description

The CMC110 is an energy measurement IC for single-phase energy metering applications. It incorporates two programmable gain amplifiers (PGAs), two ΣΔ modulators, reference circuitry, a temperature sensor, a low-dropout (LDO) regulator, a digital computation engine, and an external interface block.

The CMC110 measures 110 V or 220 V AC voltage and current applied to a load, and it calculates the corresponding power consumption and energy. In addition, it also monitors a variety of conditions such as voltage sag or swell, over-current and so on.

The CMC110 is capable of interfacing to shunt resistors, current transformers, or Hall-effect sensors for current measurement and to resistor dividers or voltage transformers for voltage measurement. It operates at a clock speed of 4.096 MHz and consumes under 15mW in 3.3 V supply.

Block Diagram



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1. Overview

The CMC110 is a single-phase energy measurement IC with an analog front end (AFE), a temperature sensor, a low-dropout (LDO) regulator, a computation engine, and an external interface block. The CMC110 measures active, reactive, and apparent power as well as RMS voltage and current. It also monitors voltage sag, voltage swell, over-current, line frequency, and various alarm status.

The AFE converts the analog voltage and current signals to digital samples and it includes two programmable gain amplifiers (PGAs) with a gain range of up to x32, reference and bias generator, and two 24-bit third-order ΣΔ modulators which output pulse density modulation (PDM) signal.

The computation engine performs the root mean square (RMS) calculation and power measurements on the voltage and current channels. The built-in calibration function calculates the calibrating gains and phases for both voltage and current channels for precise measurements and provides a simple and fast calibration scheme.

The external interface block communicates with the external micro-controller via an inter-integrated circuit (I2C), a serial peripheral interface (SPI) or a universal asynchronous receiver/transmitter (UART).

2. Applications

The CMC110 is configured to measure power in a single-phase and two-wire system. Figure 1and Figure 2 show simplified connection diagrams of the CMC110.

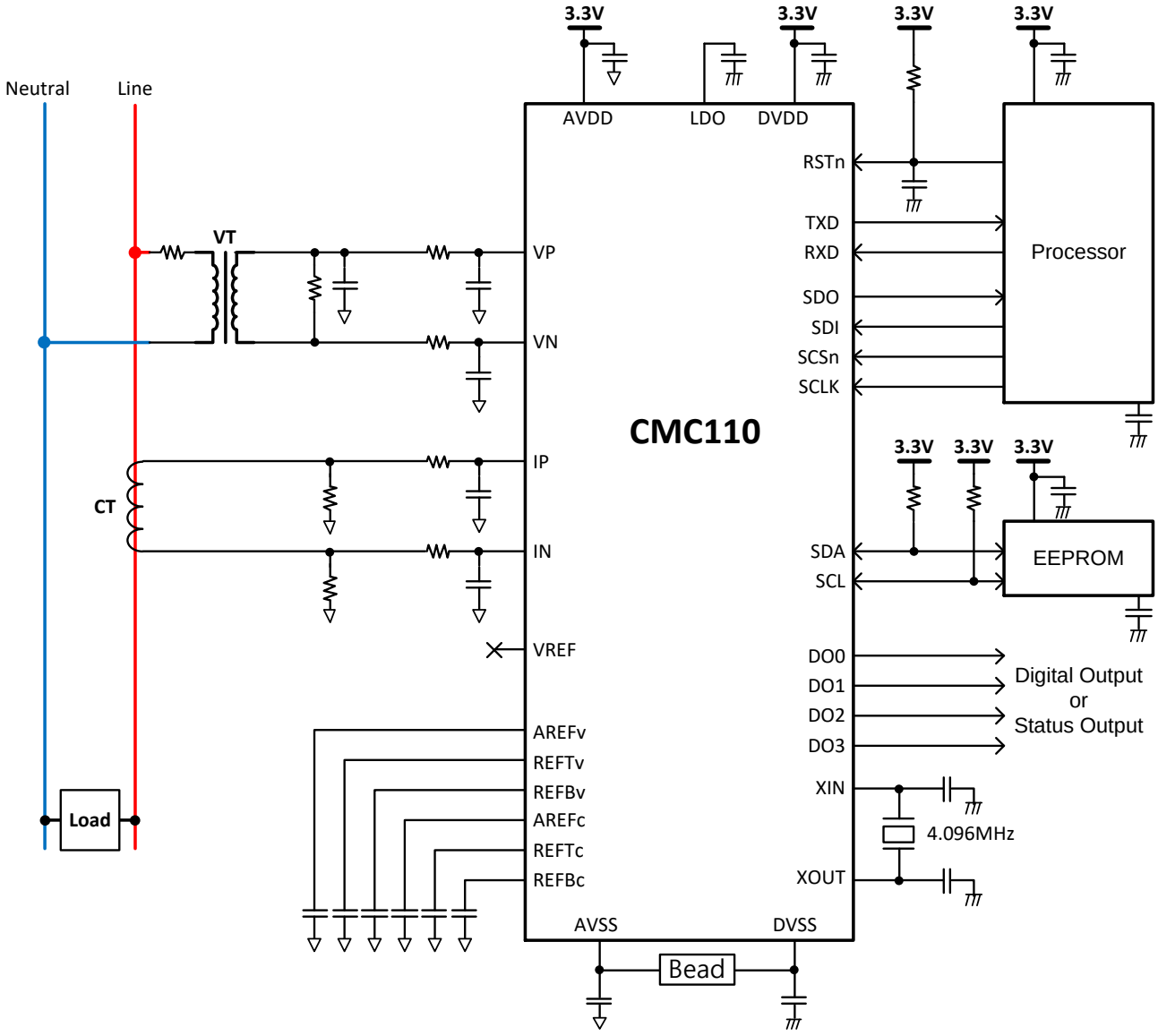

Figure 1. Connection diagram with voltage and current transformers

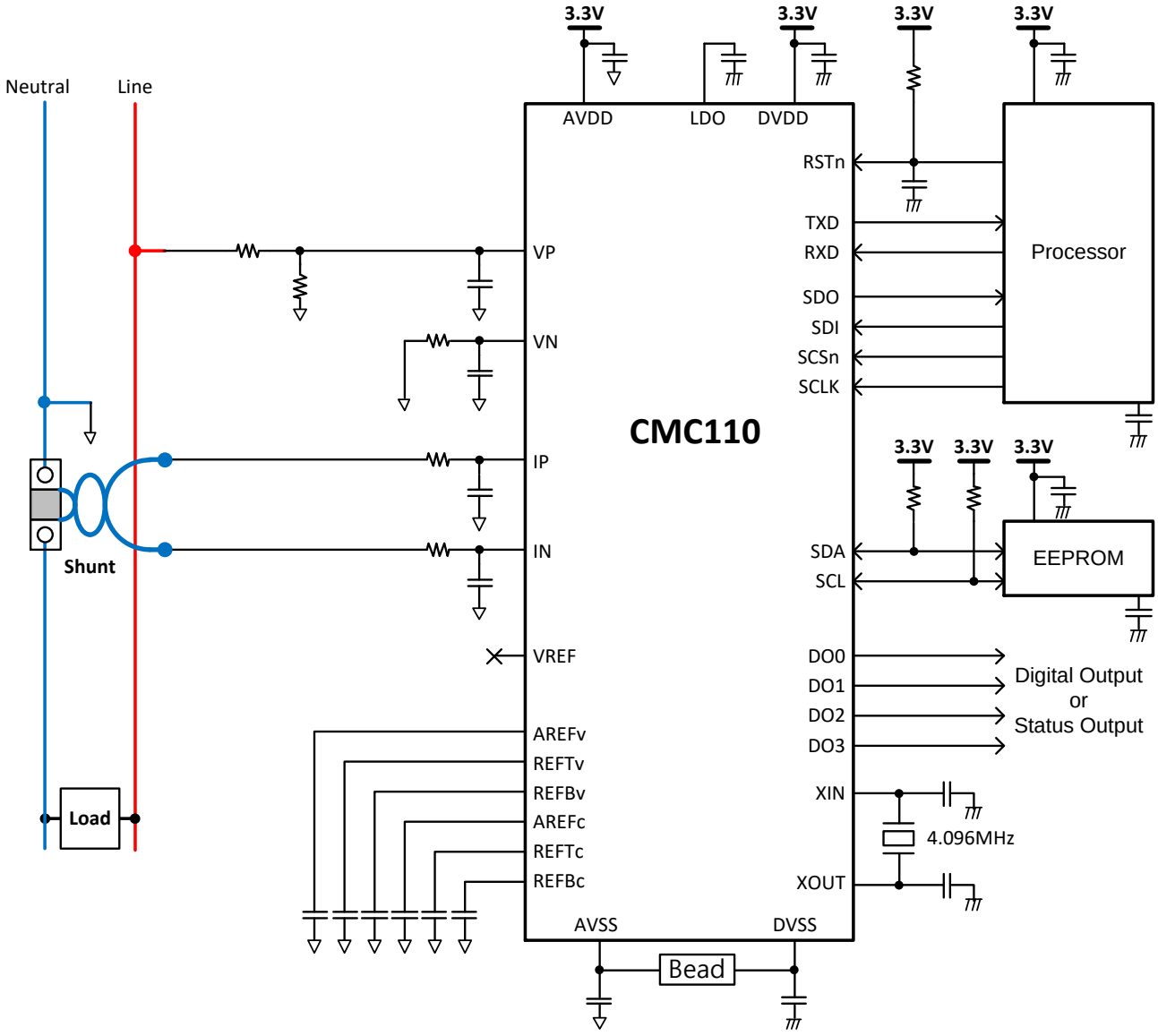

Figure 2. Connection diagram with resistor divider and shunt resistor

3. Pin Description

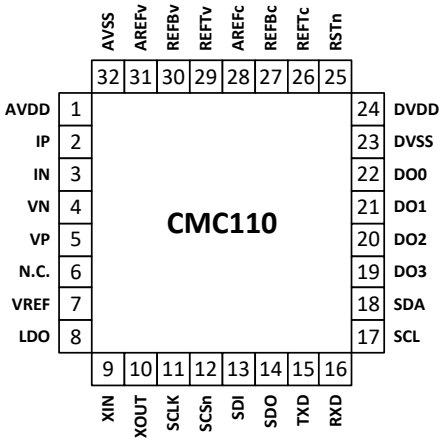

Figure 3. Pin out

Table 1. Pin Description

Pin No	Pin Name	Type[1)]	Description
1	AVDD	AI	Analog power (3.3V)
2	IP	AI	Positive analog input of current channel
3	IN	AI	Negative analog input of current channel
4	VN	AI	Negative analog input of voltage channel
5	VP	AI	Positive analog input of voltage channel
7	VREF	AO	Reference voltage output
8	LDO	AO	LDO output (1.8 V)
9	XIN	DI	Crystal input or clock input
10	XOUT	DO	Crystal output
11	SCLK	DI	SPI serial clock
12	SCSn	DI	SPI select (active low)
13	SDI	DI	SPI serial data input
14	SDO	DO	SPI serial data output
15	TXD	DO	UART transmit data
16	RXD	DI	UART receive data
17	SCL	DIO	Serial clock signal of an I^2C
18	SDA	DIO	Serial data signal of an I^2C
19	DO3	DO	Digital output
20	DO2	DO	Digital output
21	DO1	DO	Digital output
22	DO0	DO	Digital output
23	DVSS	DG	Digital ground (0 V)
24	DVDD	DP	Digital power (3.3V)
25	RSTn	DI	Reset (active low)
26	REFTc	AIO	Current channel top reference
27	REFBc	AIO	Current channel bottom reference
28	AREFc	AIO	Current channel common reference
29	REFTv	AIO	Voltage channel top reference
30	REFBv	AIO	Voltage channel bottom reference
31	AREFv	AIO	Voltage channel common reference
32	AVSS	AG	Analog ground (0 V)

1) D = Digital, A = Analog, I = In, O = Out, IO = Bidirectional, T = Tristate, P = Power, G = Ground.

4. Electrical Specifications

4.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Range	Unit
AVDD to GND	-0.3 to 4.0	V
DVDD to GND	-0.3 to 2.0	V
Ambient temperature range	-40 ~ 85	°C
Junction temperature range	-40 ~ 125	°C
Storage temperature range	-40 ~ 125	°C
ESD (HBM)	2000	V

4.2 Electrical Characteristics

Table 3. Electrical Characteristics

T_A = 25 °C, AVDD = 3.3 V, DVDD = 1.8V, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Conditions
		Min.	Typ.	Max.		
Resolution	-	-	24	-	bit	
Analog Supply Voltage	AVDD	3.0	3.3	3.6	V	
Digital Supply Voltage	DVDD	3.0	3.3	3.6	V	
Internal Reference Voltage	AVREF	-	2.7	-	V	
Input Full Scale Range	V_{FSR}	± AVREF÷GAIN			V	
Input Voltage Range	V_{IN}	± AVREF÷GAINx0.74			V	
Supply Current at Operating Mode	I_{OP}			4	mA	Simulation based
Supply Current at Power Down Mode	I_{PD}			10	uA	Simulation based
Digital Input Logic High	V_{IH}	0.7 x 1.8			V	
Digital Input Logic Low	V_{IL}			0.3 x 1.8	V	
Gain Range of PGA	G_V	1		32	V/V	
Input Clock Frequency	F_{CLK}		1		MHz	
Input Frequency Range	F_{IN}			4	kHz	
Differential Non-Linearity	DNL		TBD		LSB	
Integral Non-Linearity	INL		TBD		LSB	
Signal to Noise plus Distortion Ratio	SNDR	80	85		dB	Gain = 8, OSR = 256
		77	82			Gain = 16, OSR = 256
		75	80			Gain = 32, OSR = 256

5. Function Description

Figure 4 shows the functional block diagram of the CMC110. The functional regions are described in the following sections.

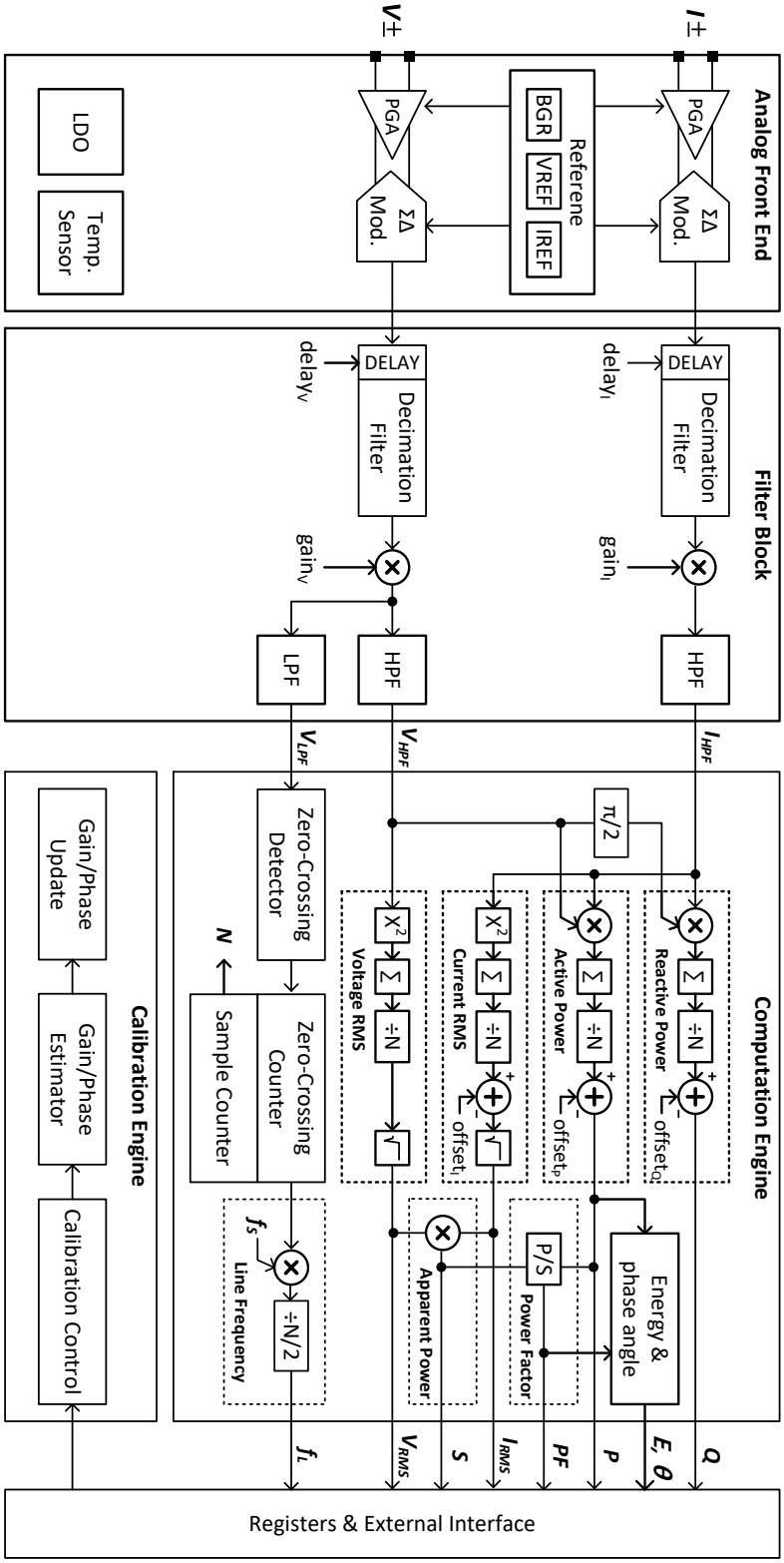

Figure 4. Functional block diagram of the CMC110

5.1 Analog Front End

The analog front end (AFE) incorporates two programmable gain amplifiers (PGAs) and two third-order ΣΔ modulators. The PGAs are interface to the voltage and current sensors and independently amplify the sensed voltage and current, respectively. Both ΣΔ modulators simultaneously convert the analog voltage and current signals to single-bit digital data streams, and sample at a rate of 1024 kHz.

5.1.1 Programmable Gain Amplifiers

The two PGAs amplify the input differential signal. They are controlled by two 3-bit GAIN registers consisting of GC_V[2:0] and GC_I[2:0]for the voltage and current channels respectively. The PGAs can be used to amplify very low signals, but the input range of the sigma-delta modulator must not be exceeded.
The following table shows the adjustable gains and the input voltage range.

No.	GC_V[2:0], GC_I[2:0]	Overall Gain		V_{IN} Range
		[V/V]	[dB]	[V]
1	000	1.0	0.0	±2.000000
2	001	2.0	6.0	±1.000000
3	010	4.0	12.0	±0.500000
4	011	5.4	14.6	±0.370370
5	100	8.0	18.1	±0.250000
6	101	10.8	20.7	±0.185185
7	110	16.0	24.1	±0.125000
8	111	32.0	30.1	±0.062500

To reduce DC offset and 1/f noise, the PGAs contain a chopping function. Its control registers are shown below. Two chopping clock signals are provided for voltage and current channels respectively.

No.	CHPENp_I, CHPENp_V	Chopping Function
1	0	Disable the chopping function.
2	1	Enable the chopping function.

No.	CHPFCp_I[1:0], CHPFCp_V[1:0]	Chopping Frequency (F_{CHF}) [MHz]
1	00	$F_{CLK}/8$
2	01	$F_{CLK}/16$
3	10	$F_{CLK}/32$
4	11	$F_{CLK}/64$

5.1.2 Sigma-Delta Modulators

The ADCs for the voltage and current channels are identical and include third-order sigma-delta modulators with a single-bit quantizer. The sampling frequency is 1 MHz with 2 MHz MCLK. The default oversampling ratio (OSR) is 128 and the maximum value is 1024.
A chopping technique is also used for the modulators. The chopping functions are controlled by CHPENs_I, CHFCs_I[2:0],CHPENs_V, and CHFC_V[2:0].The following table represents the register settings.

No.	CHPENs_I, CHPENs_V	Chopping Function
1	0	Disable the chopping function.
2	1	Enable the chopping function.

No.	CHFCs_I[2:0], CHFCs_V[2:0]	Chopping Frequency [MHz]
1	000	$F_{CLK}/2$
2	001	$F_{CLK}/4$
3	010	$F_{CLK}/8$
4	011	$F_{CLK}/16$
5	100	$F_{CLK}/32$
6	101	$F_{CLK}/64$
7	110	$F_{CLK}/128$
8	111	$F_{CLK}/256$

5.1.3 Reference and Bias Circuits

The device includes a bandgap reference. The circuit provides the reference voltage for the sigma-delta modulator.As shown in the following table, the reference voltage is selected by VCON_I[1:0] and VCON_V[1:0], and variable external reference can be applied through 26-31 pins.

No.	VCON_I[1:0], VCON_V[1:0]	Reference TOP-BOT Voltage [V]
1	00	2.70
2	01	1.00
3	10	1.65
4	11	External reference

5.1.4 LDO

This low dropout regulator provides supply voltage of 1.8 V for the core digital circuits. It is available to trim the LDO output voltage using the register, VLDO_LVL[1:0].

No.	VLDO_LVL[1:0]	LDO Output Voltage [V]
1	00	Default-0.01
2	01	Default
3	10	Default+0.01
4	11	Default+0.02

5.1.5 Temperature Sensor

The CMC110 includes an on-chip temperature sensor. Its output voltage range is controlled by TS_SCO[1:0].

No.	TS_SCO[1:0]	Output Voltage [V]			Temp. Sensor Coefficient (TSco)
		-40℃	25℃	125℃	[mV/℃]
1	00	0.957	1.330	1.554	3.622
2	01	1.194	1.702	2.008	4.933
3	10	-	-	-	-
4	11	-	-	-	-

5.2 Filter Block

The filter block consists of two decimation filters, two high-pass filters (HPFs), and a low-pass filter (LPF).

5.2.1 Decimation Filter

The single-bit sigma-delta modulator output data streams are widened to 24-bit words and down-sampled to 4 or 8 kHz with both decimation filters. The decimation filter includes a fourth-order cascaded integrator-comb (CIC) filter, a compensation filter, and a half-band (HB) filter. The CIC and compensation filters are used to achieve sampling rate decrease and compensate for the amplitude roll-off of the CIC filter, respectively. The CIC compensation filter and the HB filter are implemented using finite impulse response (FIR) filters. Figure 5 shows the frequency response of the decimation filter.

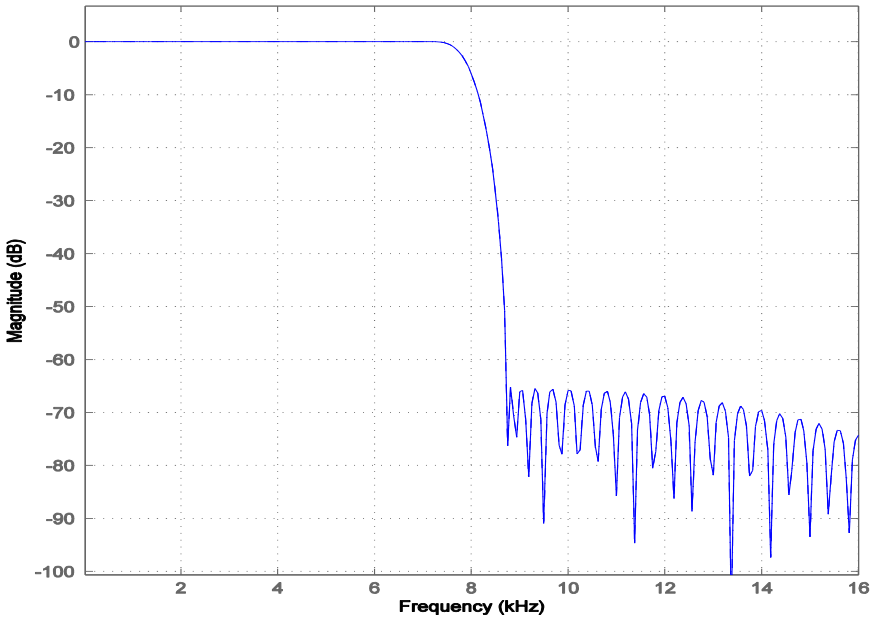

Figure 5. Frequency response of decimation filter

5.2.2 High-Pass Filter

Two HPFs remove any DC component from the voltage and current signals. The HPF is implemented using first-order infinite impulse response (IIR) filters with a cutoff frequency of 4.45 Hz. Figure 6shows the frequency response of the HPF.

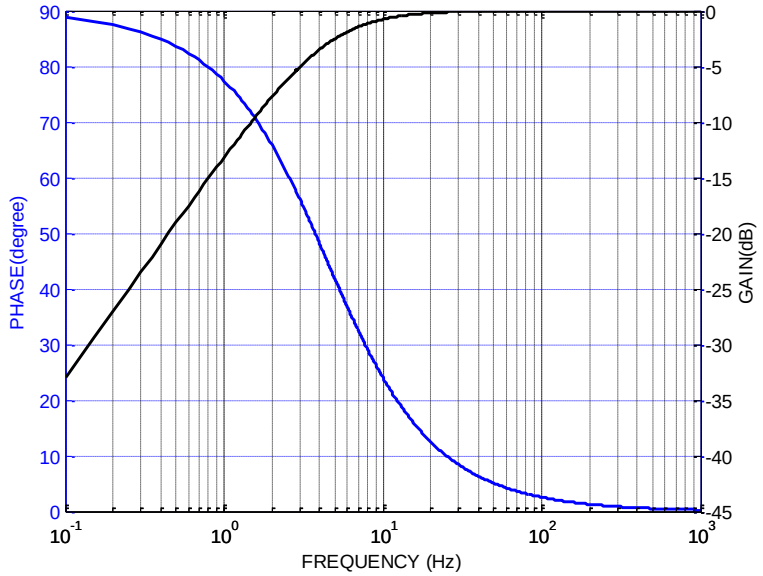

Figure 6. Frequency response of HPF

5.2.3 Low-Pass Filter

The LPF removes noise and harmonic components included in the voltage signal, and it results in a stable and accurate frequency measurement tolerant of noise and harmonics. The LPF is implemented using first-order IIR filters with a cutoff frequency of 140 Hz. Figure 7 shows the frequency response of the LPF.

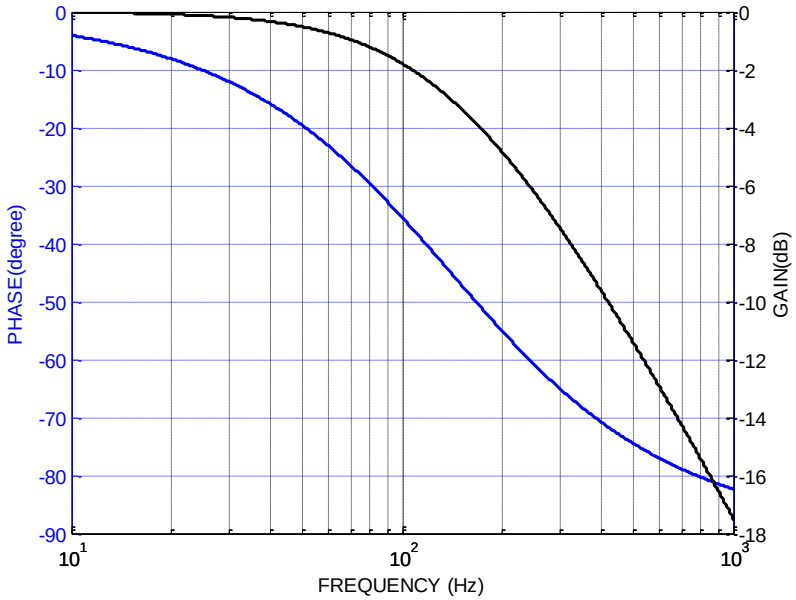

Figure 7. Frequency response of LPF

5.3 Computation Engine

The computation engine performs power measurements, line-voltage period measurement, and RMS calculation on the voltage and current. The calibration engine performs the precise estimate of errors in the gain and phase of the sensed voltage and current signals. The measured values generated from the computation engine are stored in registers.

Table 4. Measured electric power quantities

Symbol	Parameter	Equation
V_{RMS}	RMS Voltage	$V_{RMS} = \sqrt{\frac{1}{N} \times \sum_{n=0}^{N-1} v^2(n)}$
I_{RMS}	RMS Current	$I_{RMS} = \sqrt{\frac{1}{N} \times \sum_{n=0}^{N-1} i^2(n)}$
P	Active Power	$P = \frac{1}{N} \sum_{n=0}^{N-1} v(n) \times i(n)$
Q	Reactive Power	$Q = \frac{1}{N} \sum_{n=0}^{N-1} v(n - \frac{\pi}{2}) \times i(n)$
S	Apparent Power	$S = V_{RMS} \times I_{RMS} = \sqrt{P^2 + Q^2}$
PF	Power Factor	$PF = \frac{P}{S}$
P_{ACC}	Active Energy	$P_{ACC} = \sum P = P^{new} + P_{ACC}^{old}$
Q_{ACC}	Reactive Energy	$Q_{ACC} = \sum Q = Q^{new} + Q_{ACC}^{old}$
S_{ACC}	Apparent Energy	$P_{ACC} = \sum S = S^{new} + S_{ACC}^{old}$
$Angle$	Phase Angle	$Angle = cos^{-1} \frac{P}{S}$
f_L	Line Frequency	$f_L = \frac{f_S \times N_{ZC}}{N \times 2}$
Note: $v(n)$ and $i(n)$ are the instantaneous voltage and current samples, respectively. f_S is the sampling frequency, N_{ZC} is the number of zero-crossings for the voltage signal, and N is the sample count during the zero-crossing detection.		

5.3.1 RMS Calculations

RMS voltage calculation

The RMS value of the voltage (V_{RMS}) is calculated by squaring the voltage samples ($v(n)$), taking the average, and obtaining the square root. The RMS value of the voltage is defined as

$$V_{RMS} = \sqrt{\frac{1}{N} \times \sum_{n=0}^{N-1} v^2(n)}$$

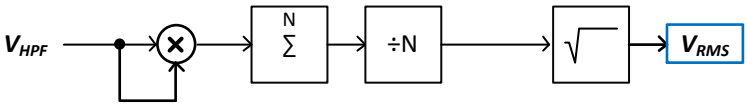

Figure 8. Voltage RMS calculation

RMS current calculation

The RMS value of the current (I_{RMS})is calculated by squaring the current samples ($i(n)$), taking the average, and obtaining the square root. The RMS value of the current is defined as

$$I_{RMS} = \sqrt{\frac{1}{N} \times \sum_{n=0}^{N-1} i^2(n)}$$

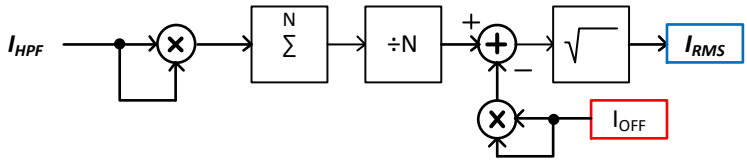

Figure 9. Current RMS calculation

5.3.2 Power Calculations

Active Power Calculation

The active power (P) is the average value of the instantaneous power which is the product of the instantaneous voltage($v(n)$) and the instantaneous current ($i(n)$)during the observation time interval. The active power is defined by

$$P = \frac{1}{N} \sum_{n=0}^{N-1} v(n) \times i(n)$$

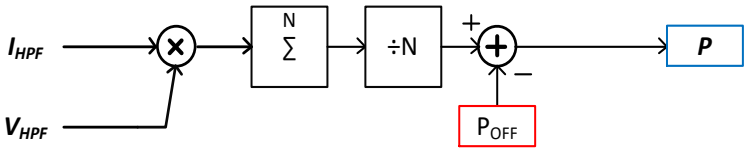

Figure 10. Active power calculation

Reactive Power Calculation

The reactive power (Q) is the average value of the instantaneous reactive power which is obtained by multiplying the instantaneous current ($i(n)$) by the instantaneous quadrature voltage ($v(n-\pi/2)$). The instantaneous quadrature voltage is obtained by phase shifting instantaneous voltage $\pi/2$ using an integrator with ω gain. ω is the angular frequency $2\pi f_L$ and f_L is the line frequency, e.g. 50 or 60 Hz. The reactive power is defined by

$$Q = \frac{1}{N} \sum_{n=0}^{N-1} v(n - \frac{\pi}{2}) \times i(n)$$

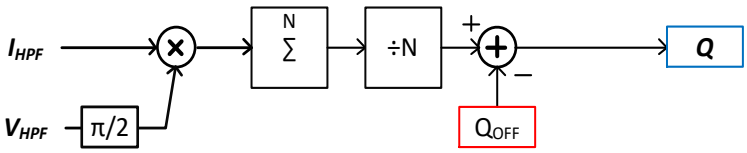

Figure 11. Reactive power calculation

Apparent Power Calculation

The apparent power (*S*) is defined as the maximum power that can be delivered to a load, and it is the product of the RMS voltage and the RMS current. The apparent power is defined by

$$S = V_{RMS} \times I_{RMS} = \sqrt{P^2 + Q^2}$$

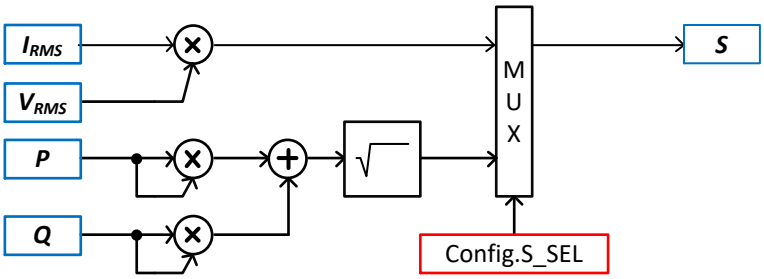

Figure 12. Apparent power calculation

Power Factor Calculation

The power factor (*PF*) is the ratio between the energy transmitted to the load over the maximum energy. It is defined as the active power divided by the apparent power. The power factor is defined by

$$PF = \frac{P}{S}$$

5.3.3Energy calculations

Active Energy Calculation

The active energy (P_{ACC}) is calculated by accumulating the active power over the time. The active energy is defined by

$$P_{ACC} = \frac{1}{3600}\sum P$$

Reactive Energy Calculation

The reactive energy (Q_{ACC}) is calculated by accumulating the reactive power over the time. The reactive energy is defined by

$$Q_{ACC} = \frac{1}{3600}\sum Q$$

Apparent Energy Calculation

The apparent energy (S_{ACC}) is calculated by accumulating the apparent power over the time. The apparent energy is defined by

$$S_{ACC} = \frac{1}{3600}\sum S$$

6. Registers

The registers are automatically reset to their default values at power up by a power-on-reset (POR).

6.1 Programming Information

The CMC110 registers are programmed using a UART, a SPI or a standard 2-wire I2C interface. The bus protocol is described in Chapter 7.

6.2 Summary

Table 5. Register Summary

Address	Name	Type	LSB	Default	Description
00	Reserved				
01	f_L	RO	0.01 Hz		Line frequency [Hz].
02	Alarm Status	RO			Alarm status.
03	CNT_I_{RMS}_over	RO	1		Over-current event counter.
04	CNT_V_{RMS}_under	RO	1		Under-voltage event counter.
05	CNT_V_{RMS}_over	RO	1		Over-voltage event counter.
06	V_{RMS}	RO	mV		RMS voltage measurement [V_{RMS}].
07	I_{RMS}	RO	mA		RMS current measurement [A_{RMS}].
08	P	RO	mW		Active power measurement [W].
09	Q	RO	mVAR		Reactive power measurement [VAR].
0A	S	RO	mVA		Apparent power measurement [VA].
0B	PF	RO	0.001		Power Factor. The output is between -0.999 to 1.000.
0C	Phase Angle	RO	0.001		Phase Angle between voltage and current [Degree]. The output is between -179.999 and +180.000.
0D	Reserved				
0E	Reserved				
0F	Reserved				
10	Imported P_{ACC}	RO	mWh		Imported active energy [Wh].
11	Exported P_{ACC}	RO	mWh		Exported active energy [Wh].
12	Imported Q_{ACC}	RO	mVARh		Imported reactive energy [VARh].
13	Exported Q_{ACC}	RO	mVARh		Exported reactive energy [VARh].
14	Q_{ACC}	RO	mVARh		Reactive energy [VARh].
15	S_{ACC}	RO	mVAh		Apparent energy [VAh].
16	PF_{AVG}	RO	0.001		Averaged power factor. The output is between -0.999 to +1.000.
17	Reserved				
18	Reserved				
19	Reserved				
1A	Reserved				
1B	Reserved				
1C	Reserved				
1D	Reserved				
1E	Reserved				
1F	Reserved				

Address	Name	Type	LSB	Default	Description
20	MIN_{VRMS}	RO	mV		Minimum V_{RMS} measured
21	MAX_{VRMS}	RO	mV		Maximum V_{RMS} measured
22	MIN_P	RO	mW		Minimum active power measured
23	MAX_P	RO	mW		Maximum active power measured
24	MIN_{IRMS}	RO	mA		Minimum I_{RMS} measured
25	MAX_{IRMS}	RO	mA		Maximum I_{RMS} measured
26	MIN_Q	RO	mW		Minimum reactive power measured
27	MAX_Q	RO	mW		Maximum reactive power measured
28	MIN_S	RO	mW		Minimum apparent power measured
29	MAX_S	RO	mW		Maximum apparent power measured
2A	MIN_{PF}	RO	0.001		Minimum power factor measured
2B	MAX_{PF}	RO	0.001		Maximum power factor measured
2C	MIN_{ANGLE}	RO	0.001		Minimum phase angle measured
2D	MAX_{ANGLE}	RO	0.001		Maximum phase angle measured
2E	Reserved				
2F	CNT_{SYS}	RO	Sec		System Counter
30	V_n	RO			Instantaneous Voltage
31	$V90_n$	RO			Instantaneous Quadrature Voltage
32	I_n	RO			Instantaneous Current
33	P_n	RO			Instantaneous Active Power
34	Q_n	RO			Instantaneous Reactive Power
35	Reserved				
36	Reserved				
37	Reserved				
38	Reserved				
39	Reserved				
3A	Reserved				
3B	V_{PEAK}	RO			Peak Voltage
3C	I_{PEAK}	RO			Peak Current
3D	Reserved				
3E	Reserved				
3F	Reserved				
40~4F	Reserved				
50~5F	Reserved				
60~6F	Reserved				
70~7F	Reserved				
80	$Gain_V$	RW		1000 0000h	Calibrating gain for voltage channel
81	$Gain_I$	RW		1000 0000h	Calibrating gain for current channel
82	$Gain_P$	RW		1000 0000h	Calibrating gain for active power
83	$Gain_Q$	RW		1000 0000h	Calibrating gain for reactive power
84	$Gain_S$	RW		1000 0000h	Calibrating gain for apparent power
85	Reserved				
86	DC_V	RW		0000 0000h	Calibrating DC offset for voltage channel
87	DC_I	RW		0000 0000h	Calibrating DC offset for current channel
88	$DELAY_{V,I}$	RW		0000 0000h	Calibrating delays for voltage and current channels
89	$OFFSET_I$	RW		0000 0000h	Calibrating offset for RMS current
8A	$OFFSET_P$	RW		0000 0000h	Calibrating offset for active power
8B	$OFFSET_Q$	RW		0000 0000h	Calibrating offset for reactive power
8C	Reserved				
8D	Reserved				
8E	V_{MAX}	RW	mVrms	+471.500d	External maximum RMS voltage [V_{RMS}]
8F	I_{MAX}	RW	mArms	+52.000d	External maximum RMS current [I_{RMS}]

Address	Name	Type	LSB	Default	Description
90	I_{MIN}	RW	mArms	+0.007d	External starting RMS current [I_{RMS}].
91	P_{MIN}	RW	mW	+0.010d	External starting active power [W]
92	Q_{MIN}	RW	mVAR	+0.010d	External starting reactive power [VAR]
93	VCAL	RW	mVrms	+220.000d	Target line voltage for calibration [V_{RMS}]
94	ICAL	RW	mArms	+1.000d	Target load current for calibration [I_{RMS}]
95	PCAL	RW	mW	+220.000d	Target active power for calibration [W]
96	PHCAL	RW	0.001	+0..010d	Target phase angle for calibration [degree]
97	Reserved				
98	Reserved				
99	V_{TOL}	RW	mVrms	+0.100d	Tolerance on RMS voltage for calibration [V_{RMS}]
9A	I_{TOL}	RW	mArms	+0.100d	Tolerance on RMS current for calibration [I_{RMS}]
9B	P_{TOL}	RW	mW	+0.100d	Tolerance on active power for calibration [W]
9C	PH_{TOL}	RW		+0.050d	Tolerance on phase angle for calibration [degree]
9D	Reserved				
9E	$CNT1_{CAL}$	RW		1E1E030Ah	Calibration count1
9F	$CNT2_{CAL}$	RW		03E8 03E8h	Calibration count2
A0	CONFIG	RW		0873 0035h	Configuration register
A1	MODE	RW		0006 33FFh	Mode register
A2	CNT_{SMAPLE}	RW		4000d	Average sample count for averaged electric quantities
A3	CNT_{CYCLE}	RW		120d	Average cycle count for averaged electric quantities
A4	CNT_{ZC}	RW		120d	Zero-crossing count for line frequency measurement
A5	$LEVEL_{ZC}$	RW		0010 0000h	Zero-crossing level
A6	Reserved				
A7	$MODE_{GPIO}$			0000 0000h	Digital output configuration
A8	T_{AUTO}	RW		0000 0001h	Auto-report timer
A9	REPORT0	RW		0908 0706h	Register selection for auto-report message
AA	REPORT1	RW		010B 100Ah	Register selection for auto-report message
AB	REPORT2	RW		FFFF FFFFh	Register selection for auto-report message
AC	REPORT3	RW		FFFF FFFFh	Register selection for auto-report message
AD	AFE0	RW		00C4 6C11h	AFE mode register
AE	AFE1	RW		00C4 6C11h	AFE mode register
AF	AFE2	RW		0000 0201h	AFE mode register
B0	$LEVEL\_MIN_f$	RW		+59.00d	Minimum line frequency alarm threshold
B1	$LEVEL\_MAX_f$	RW		+61.00d	Maximum line frequency alarm threshold
B2	$LEVEL\_V_{PEAK}$	RW		+80.000d	Maximum peak voltage alarm threshold
B3	$LEVEL\_MIN_{VRMS}$	RW		+200.000d	Minimum RMS voltage alarm threshold
B4	$LEVEL\_MAX_{VRMS}$	RW		+240.000d	Maximum RMS voltage alarm threshold
B5	$LEVEL\_MAX_{IRSM}$	RW		+15.000d	Maximum RMS current alarm threshold
B6	$LEVEL\_MIN_{PF}$	RW		-0.700d	Minimum power factor alarm threshold
B7	$LEVEL\_MAX_{PF}$	RW		+0.700d	Maximum power factor alarm threshold
B8	Reserved				
B9	Reserved				
BA	$MASK_{ALARM}$	RW		7010 197Ch	Alarm mask
BB	Reserved				
BC	Reserved				
BD	Reserved				
BE	Reserved				
BF	Reserved				
C0	CMD0	RW		0000 0000h	Command register
C1	CMD1	RW		0000 0000h	Command register
C2	CMD2	RW		0000 0000h	Command register
C3-CF	Reserved				
D0-FF	Reserved				

7. External Interface

7.1 UART interface

The CMC110 provides a two-wire, asynchronous, full-duplex UART port. The CMC110 UART operates in 8-bit mode. Data is transmitted and received LSB first, with one start bit, eight data bits, and one stop bit. The default configuration is 38400 baud, no-parity, 1 stop-bit, and no flow control. The UART has two signals such as TXD and RXD. TXD is the serial data output from the CMC110. RXD is the serial data input to the CMC110.

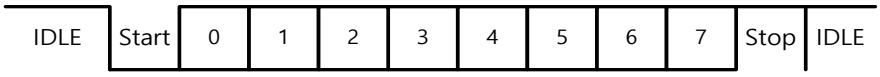

Figure 13. UART interface

UART Commands

Commands	Description	Example
)reg_addr$<CR>	Read the register in hex	)A0$<CR>
)reg_addr?<CR>	Read the internal register in decimal	)8E?<CR>
)reg_addr=n<CR>	Write the value n to address reg_addr in hex format	)A0=0123F8F0<CR>
)reg_addr=+n<CR>	Write the value n to address reg_addr in decimal format	)8E=+471.5<CR>

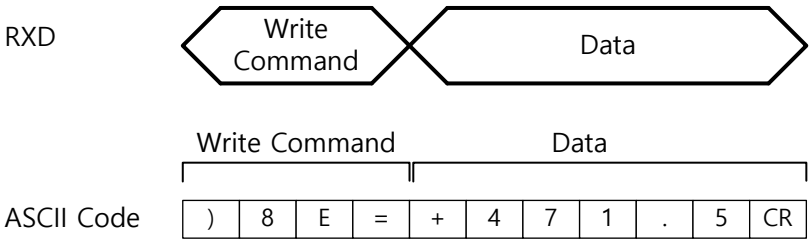

Figure 14. UART interface: register write operation

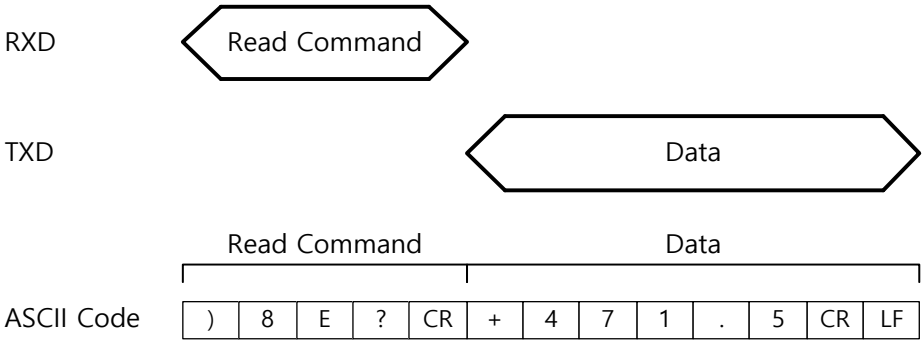

Figure 15. UART interface: register read operation

7.2 I2C interface

The CMC110 I2C can be configured as a master and a slave. The CMC110 I2C automatically operates at boot time to load configuration information from an external I2C device. The I2C has two signals such as SDA and SCL. SDA and SCL are the serial data bus and the serial clock, respectively.

Device Operation

- **Data Transitions:** The SDA changes only during the SCL is low.
- **Start Condition:** A high to low transition of the SDA is a start condition while the SCL is high.
- **Stop Condition:** A low to high transition of the SDA is a stop condition while the SCL is high.
- **Acknowledge:** All addresses and data words are serially transmitted to and from the CMC110 in 8-bit words. The CMC110 sends an acknowledge bit during the 9th clock cycle of the SCL. When the CMC110 has received each 8-bit word, the CMC110 sends a zero (ACK).

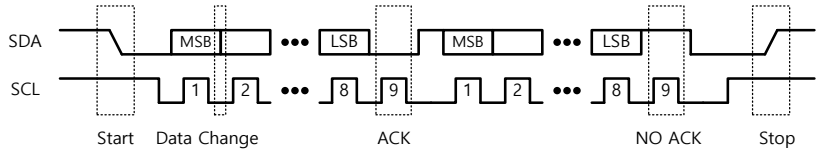

Figure 16. I2C device operation

Device Addressing

The CMC110 requires an 8-bit device address word following a start condition to enable the CMC110 for a read or write operation. The device address word consists of 7-bit device address bits and a 1-bit read/write select bit. The read or write operation is initiated when the 8th bit of the device address is high or low, respectively.

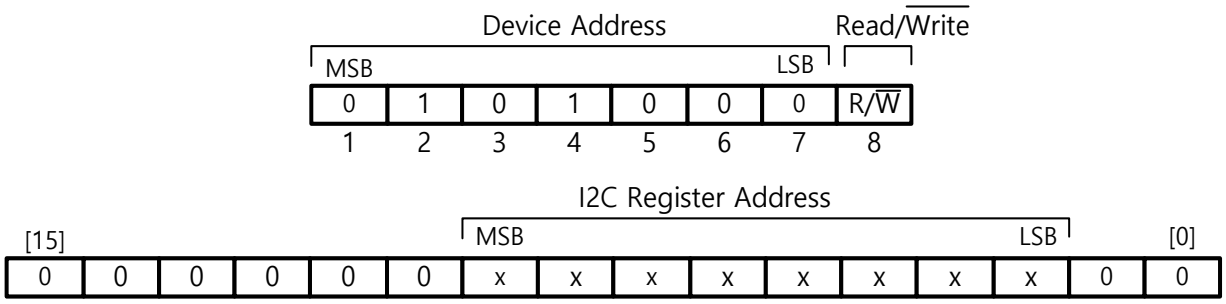

Figure 17. I2C device addressing & Register addressing

Write Operations

- **Random Write:** A random write operation requires an 8-bit register address following the 8-bit device address word and a 1-bit acknowledge bit. The four data bytes are required to be written into the addressed register location of the CMC110. The write operation ends when a stop condition is generated by an external I2C master.
- **Sequential Write:** A sequential write operation is initiated the same way as a random write operation. However, a stop condition is not sent after the first four data bytes are written into the addressed register location. The 32-bit data words can be written into the internal registers of the CMC110 until a stop condition is generated. The internal register pointer will be incremented when receiving a stop condition.

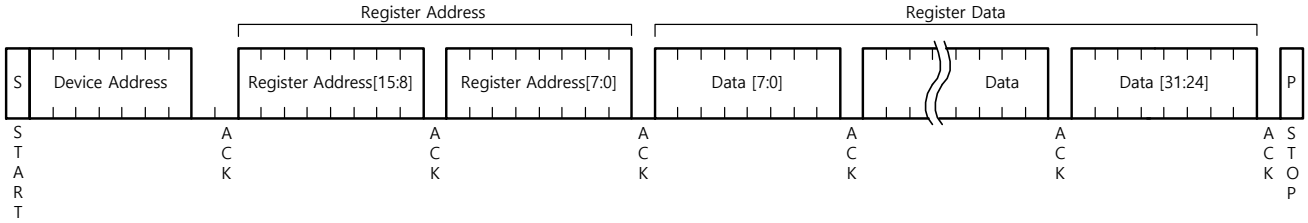

Figure 18. I2C interface: random write operation

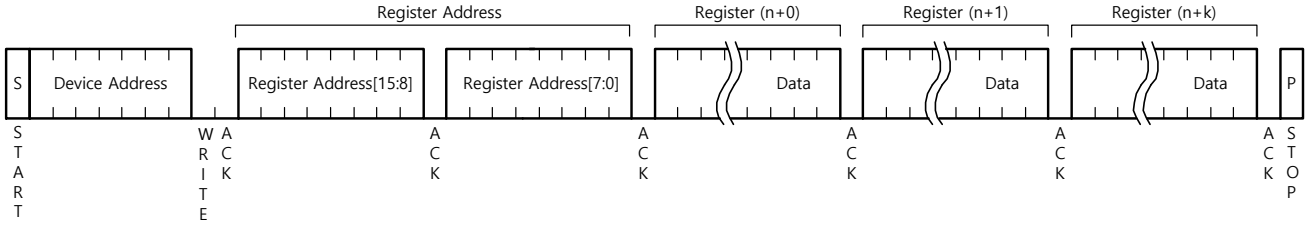

Figure 19. I2C interface: sequential write operation

Read Operations

- **Current Address Read:** The internal address counter maintains the last address accessed during the last read or write operation, incremented by one. After the device address with the read/write select bit set to one is clocked in and acknowledged by the CMC110, four 8-bit data are serially clocked out. An external I2C master responds with ACK for the first three 8-bit data. When the 4th 8-bit data is read, the external I2C master responds with NO ACK and generates a stop condition.
- **Random Read:** After the device address and the register address are clocked in and acknowledged by the CMC110, another start condition must be generated by the external I2C master. A current address read is initiated by a device address with the read/write select bit high. The CMC110 acknowledges the device address and serially clocks out the four 8-bit data.
- **Sequential Read:** A sequential read operation is initiated the same way as a random read operation. However, a stop condition is not sent after the first four data bytes are read from the addressed register location. The 32-bit data words can be read from the internal registers of the CMC110 until a stop condition is generated. The internal register pointer will be incremented when receiving a stop condition.

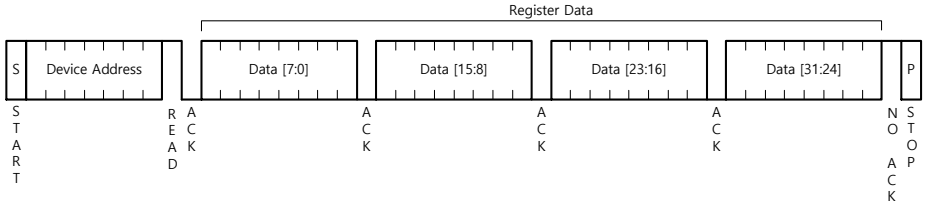

Figure 20. I2C interface: current address read operation

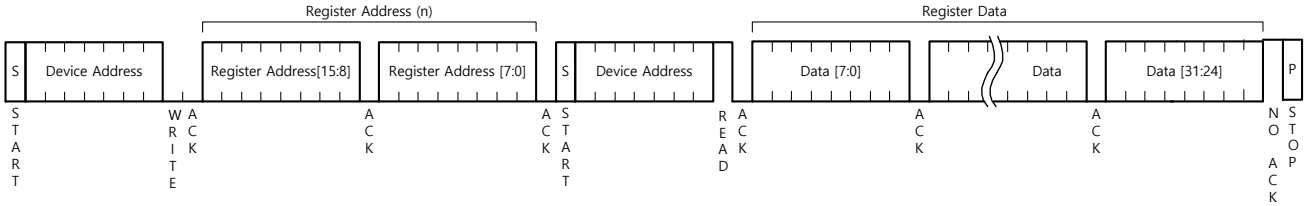

Figure 21. I2C interface: random read operation

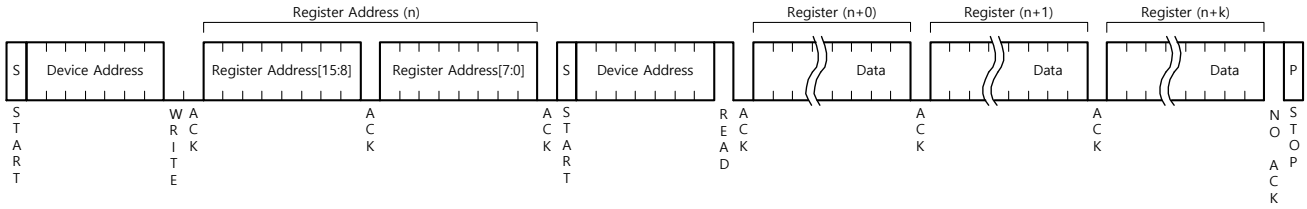

Figure 22. I2C interface: sequential read operation

7.3 SPI interface

The CMC110 SPI can be configured as a slave only. Four pins are associated with the interface as below.

- SCLK : SPI Serial Clock Input
- SCSn: SPI Chip Select
- SDI : SPI Serial Data Input (Master Input/Slave Output; MISO)
- SDO : SPI Serial Data Output (Slave Output/Master Input; MOSI)

The SPI read or write transaction is SCSn-low defined. Each transaction can access internal registers in the CMC110. Data on SDI is shifted into the CMC110 on the rising edge of SCLK while data on SDO is shifted out of the CMC110 on the falling edge of SCLK. The first bit on SDI defines the access type such as read and write. ADDR[14:0] is decoded as address

Byte Number	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	RD/WRn	ADDR[14:8]						
1	ADDR[7:0]							
2	DATA[31:24]							
3	DATA[23:16]							
4	DATA[15:8]							
5	DATA[7:0]							

Write Operations

- **Random Write:** A random write operation requires a 1-bit read/write select bit, a 15-bit register address, and four data bytes. The four data bytes are required to be written into the addressed register location of the CMC110.
- **Sequential Write:** A sequential write operation is initiated the same way as a random write operation. The 32-bit data words can be written into the internal registers of the CMC110 during SCSn is low. The internal register pointer is automatically incremented after the 32-bit data word is written into the internal register.

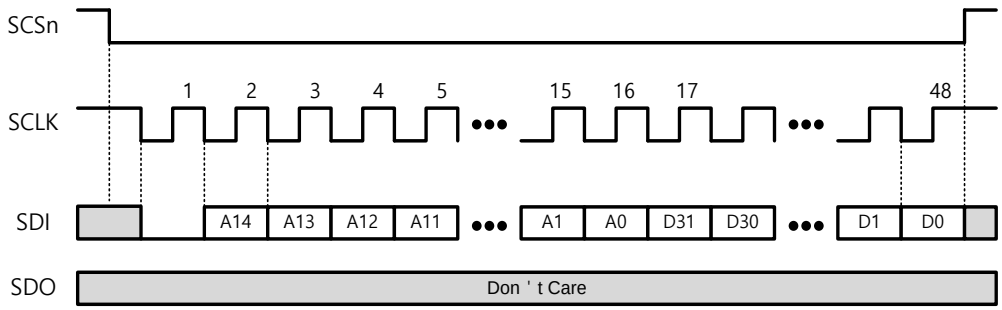

Figure 23. SPI interface: random write operation

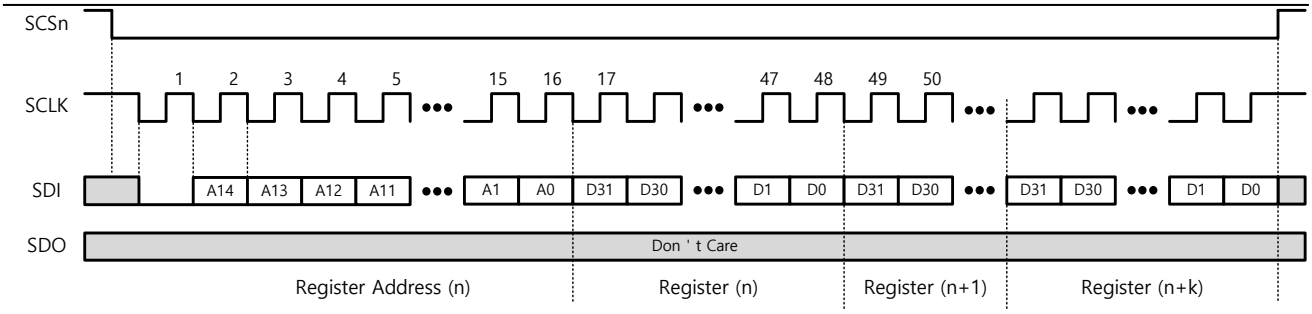

Figure 24. SPI interface: sequentialwrite operation

Read Operations

- **Random Read:** After the 1-bit read/write select bit and the 15-bit register address are clocked in, the CMC110 serially clocks out the 32-bit data word.
- **Sequential Read:** A sequential read operation is initiated the same way as a random read operation. The 32-bit data words can be read from the internal registers of the CMC110 during SCSn is low. The internal register pointer is automatically incremented after the 32-bit data word is read from the internal register.
- **Indirect Addressing Read:** An indirect addressing read operation is similar to the sequential read operation. REPORT0(A9h), REPORT1(AAh), REPORT2(ABh), and REPORT3(Ach) registers contain addresses of the internal registers which contain 32-bit data words. If an external SPI master reads a 32-bit data word from register locations whose A11 bit is '1', the CMC110 generates the 32-bit data words from the internal registers which are addressed by REPORT0, REPORT1, REPORT2, and REPORT3 registers. Figure 25 shows the block diagram of an address generator for the indirect addressing read operation.
-

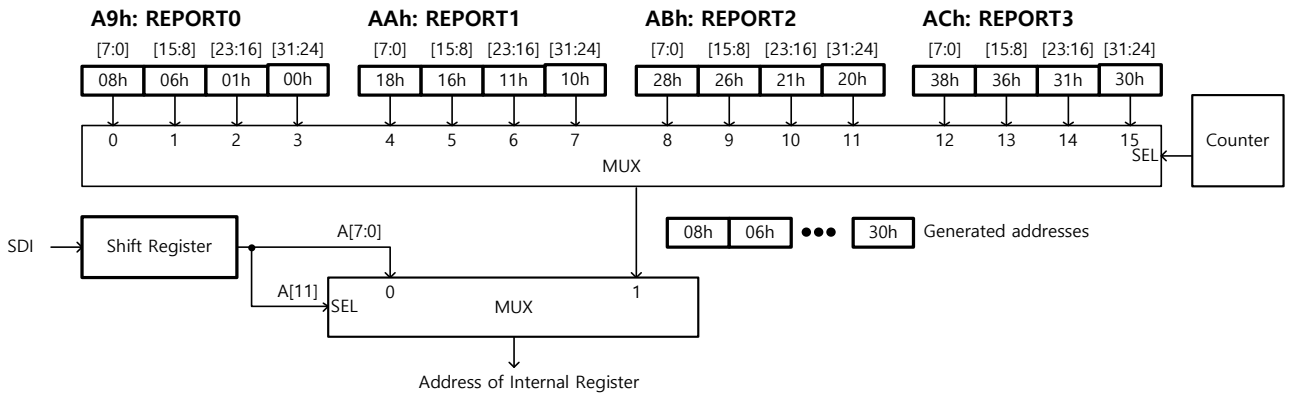

Figure 25. Block diagram of address generator for indirect addressing read operation

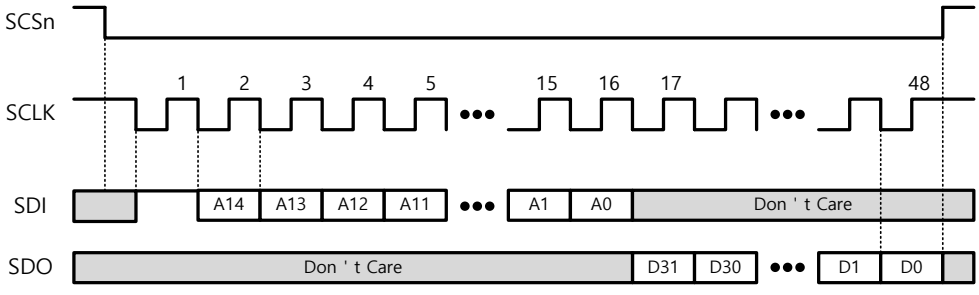

Figure 26. SPI interface: random read operation

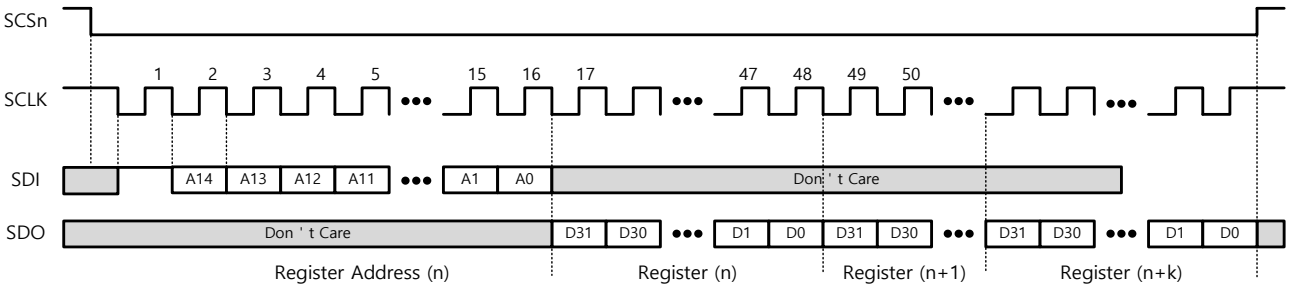

Figure 27. SPI interface: sequential read operation

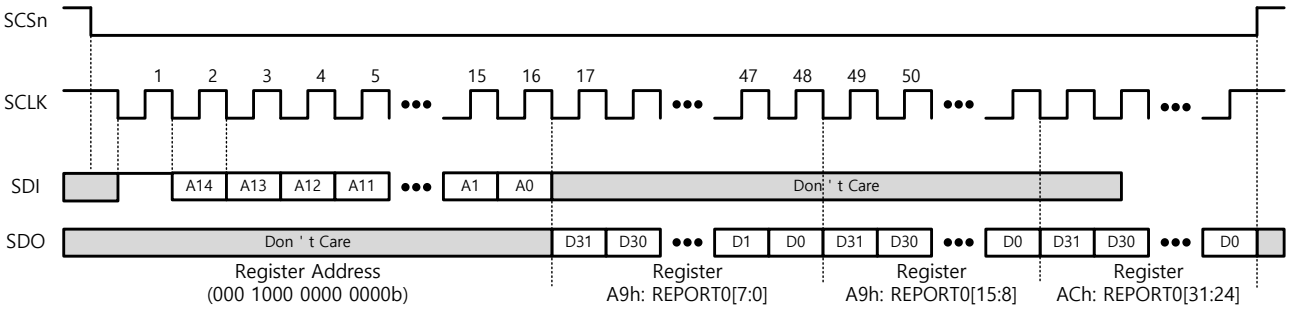

Figure 28. SPI interface: indirect addressing read operation

8. System Calibration

The CMC110 provides a built-in calibration function for a simple and fast calibration. Figure 29 shows the gain and phase calibration scheme. The calibration engine calculates the calibrating gains and delays for both voltage and current channels using the measured values generated from the computation engine. The calibrating gains and delays are used to compensate both the voltage and current signals.

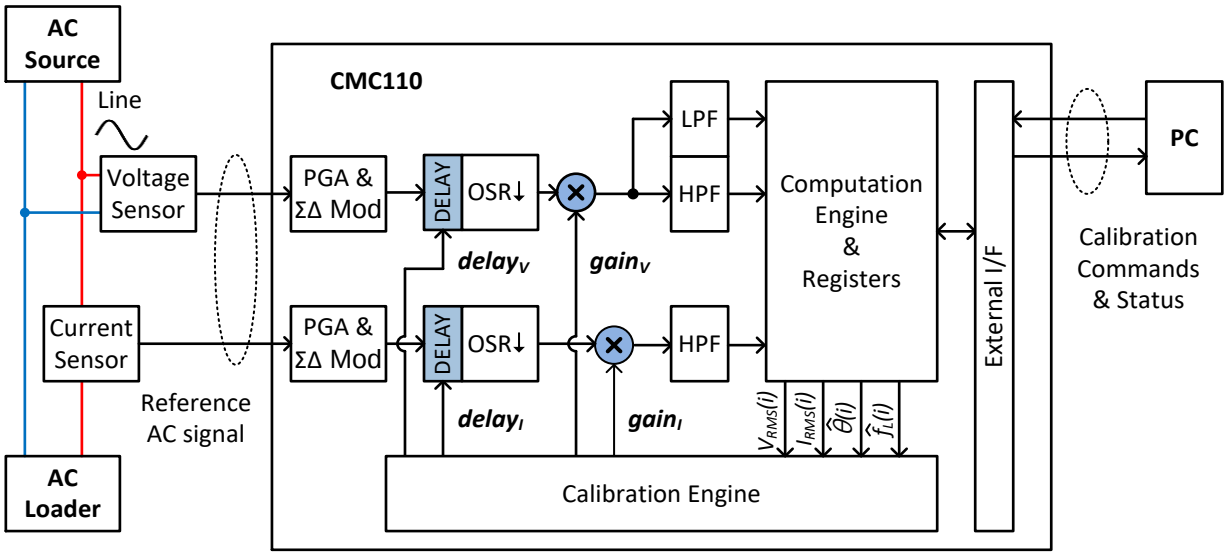

Figure 29. Gain and phase calibration scheme

8.1 Gain Calibration

The gain calibration procedure is as follows. First, a reference AC signal must be applied to the channel to be calibrated. After the computation engine operation, the measured RMS voltage is stored in the register. The calibration engine estimates the RMS voltage error and calculates the calibrating gain. The gain calibration procedure is performed repeatedly until the estimated error is less than the tolerance value or the iteration count is equal to the predefined maximum iteration value. The current gain calibration is simultaneously performed with the same method of the gain calibration.

8.2 Phase Calibration

The phase calibration is similar to the gain calibration. First, a reference AC signal must be applied to the channel to be calibrated. After the computation engine operation, a measured power factor and a measured line frequency are stored in the internal registers. The calibration engine estimates the phase difference between the voltage and current and calculates the corresponding delay using the measured power factor and the measured line frequency. If the absolute value of the estimated phase is greater than the predefined tolerance value and the iteration count is less than the predefined maximum iteration value, the iteration count is increased by one. And if the estimated phase is a positive value, the calibrating delay for the voltage channel is updated. Otherwise, the calibrating delay for the current channel is updated.

9. Package Dimensions

The CMC110 is packaged in a 32-pin quad-flat no-leads (QFN) package. Figure 30 below shows the package outline and the dimensions.

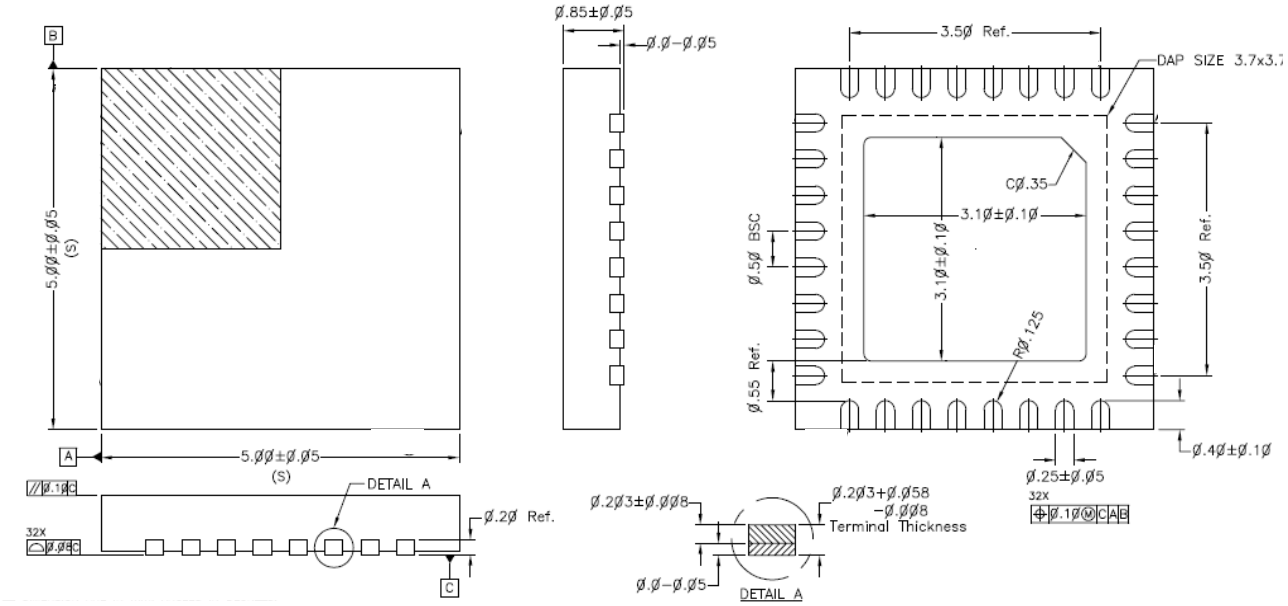

Figure 30. 32 QFN package drawing

10. Revision History

Version	Date	Description
Preliminary	2014-11-16	Preliminary
Rev. 0.2b	2016-02-29	
Rev. 0.3d	2016-08-05	Updated the I2C protocol.
Rev. 0.3e	2016-09-01	Updated the package information.
Rev. 0.4a	2016-09-30	Updated the pin description.
Rev. 0.4b	2016-11-23	Fixed typo.
Rev. 0.4c	2017-03-31	Revised register table in 6.2.
Rev. 0.4d	2021-03-26	Revised PGA Gain in table 3.